UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Offic
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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|---|---|---|---|
| 09/229,592 | 01/13/99 | DOYLE B | 42390.P5578 |

MM92/1221

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| **ART UNIT** | **PAPER NUMBER** |
| 2815 | |

**DATE MAILED:** 12/21/00

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trad marks**

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/229,592 | DOYLE ET AL. | |
| | Examiner | Art Unit | |
| | Paul E Brock II | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

**Attachment(s)**

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1 – 6 and 8 – 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Rodder et al.

With regard to claim 1, Rodder et al. disclose a method of forming a transistor in figures 3a – 5. In figure 3a Rodder et al. disclose forming an alignment component (120) on a substrate (102) of a semiconductor material. Rodder et al. discloses in figure 3b and column 3, lines 5 – 40 forming raised source/drain regions using salicidation. It is inherent that the salicidation technique would include depositing a metal layer over the substrate and the alignment component, and reacting the metal layer with the semiconductor material of the substrate to form two silicide regions (106) substantially extending up to the alignment component on opposing sides of the alignment component. In figures 3e – 5 and column 5, lines 11-26 Rodder et al. discloses replacing the alignment component with a conductive gate (112) substantially extending up to the silicide regions.

With regard to claims 2 – 4, Rodder et al. discloses in columns 2 and 3, lines 59 – 67 and 1- 4 respectively that the alignment component is made of silicon oxide which inherently posses

the properties of being non-conductive, and will not react with the metal layer when the metal layer is reacted with the semiconductor material of the substrate.

With regard to claims 5, 6 and 8, Rodder et al. discloses in column 2, lines 11 – 17 that the alignment component is less than .10 microns wide. It is inherent that the alignment component has a thickness of between 1000Å and 2500Å. It is inherent that the metal layer is between 300Å and 400Å thick.

With regard to claim 9, it is an inherent property of salicidation that the silicide regions formed have lower surfaces located lower than a lower surface of the alignment component, and inner surfaces, facing one another, which are in contact with the semiconductor material of the substrate.

With regard to claim 10, Rodder et al. discloses in figures 3c – 5 a method whereby the alignment component is replaced with the gate. In figure 3c Rodder et al. discloses depositing a layer (114) over the silicide regions and the alignment component. In column 3, lines 46 – 49 Rodder et al. discloses planarizing the layer at least until the alignment component is exposed. In figures 3e and 3f Rodder et al. discloses etching the alignment component to leave an opening in the first layer. In figures 3g – 5 Rodder et al. discloses disposing a gate within the opening.

With regard to claim 11, in figure 3f Rodder et al. discloses after etching of the alignment component, the silicide regions extend substantially up to the opening.

With regard to claim 12, Rodder et al. discloses in columns 2 and 3, lines 59 – 67 and 1 – 52 respectively the alignment component and the layer are made of different materials, one being made of silicon oxide and the other being made of silicon nitride.

With regard to claims 13 and 14, Rodder et al. discloses in figure 5, and column 4, lines 56 – 67 depositing a gate dielectric layer (110), and forming a gate electrode on the gate dielectric layer. It is inherent that the gate dielectric is less than 10Å Thick.

With regard to claim 15, Rodder et al. discloses in column 4, lines 42 – 55 that the gate electrode is made out of a metal.

With regard to claim 16, Rodder at al. discloses in figure 4 forming doped regions (104) which extend from the silicide regions in underneath the gate.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder et al. as applied to claim 1 above, and further in view of Sekine et al.

Rodder et al. does not disclose a material for the metal layer. Sekine et al. discloses in column 1, lines 31 – 44 using titanium for forming a metal layer in the process of making a silicide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use titanium as a metal layer in the process for forming a transistor of Rodder et al. in order to decrease the resistance of the electrode portions as stated by Sekine et al. in column 1, lines 36 – 44.

5. Claims 17 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder et al. as applied to claim 1 and 13 above, and further in view of Gardner et al. (USPAT 6051865).

With regard to claims 17 and 18, Rodder et al. does not disclose using a high K dielectric layer. Gardner et al. (USPAT 6051865) teaches in columns 3 and 4, lines 24 – 40 and 24-36 respectively a gate dielectric layer of barium strontium titanate that has a dielectric constant of at least 100. It would have been obvious to one of ordinary skill in the art at the time of the present invention in order to decrease the transistor threshold voltage as stated by Gardner et al. (USPAT 6051865) in column 3, lines 26 – 33.

With regard to claim 19, Rodder et al. in view of Gardner et al. (USPAT 6051865) does not disclose using platinum as a gate electrode. It is well known in the art to form a gate electrode of platinum. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the platinum gate electrode in the process of forming a transistor of Rodder et al. in view of Gardner et al. (USPAT 6051865) in order to use a low-resistivity conductor for the gate material.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Inumiya et al. discloses forming silicide regions, removing a dummy gate and replacing it with a gate electrode. Saxena teaches the use of platinum electrodes. Hieda, Chan et al., Sato, Masuoka, Ang et al., Gardner et al. (USPAT 6103559), Gardner et al. (USPAT 5994193), and Iranmanesh et al. all teach of removing at least part of a dummy gate and replacing it with a gate electrode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
December 12, 2000

EDDIE C. LEE
PRIMARY EXAMINER